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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/755,546      | 01/12/2004  | Patrick Y. Huet      | 58843.US            | 1307             |

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| EXAMINER |
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CABRERA, ZOILA E

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| ART UNIT | PAPER NUMBER |
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2125

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/755,546

Applicant(s)

HUET ET AL

Examiner

Zoila E. Cabrera

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 6, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by **Dor et al. (US 6,701,259)**.

Regarding claims 1-2 and 11, **Dor** discloses a method for analyzing defects on a substrate or semiconductor substrate, the method including the steps of:

- optically inspecting the substrate to detect the defects (Col. 6, lines 5-15)),  
inspecting the substrate to detect the defects (Col. 6, lines 7-12),  
identifying the defects by location (Col. 6, lines 43-46; Col. 15, lines 18-20),  
analyzing the defects to detect extended objects (Col. 6, lines 56-58; i.e., cluster corresponds to extended objects as defined in Specification page 7, lines 14-15),  
and analyzing the extended objects for repetition across the substrate (Col. 13, lines 60-65, i.e., the **clusters** of defect are highlighted on the wafer map).

As for claims 6 and 12, Dor further discloses

- the extended objects include at least one of clusters and signatures (Col. 17, lines 6-11 and lines 49-55)

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dor et al. (US 6,701,259)** in view of **Ninomiya (US 2002/0035435 A1)**.

Regarding claim 17, **Dor** further discloses an apparatus for analyzing defects on a substrate the apparatus comprising:

a sensor for inspecting the substrate (Fig. 1, metrology tools include sensors; Col. 3, lines 25-31); and  
a controller (Col. 5, lines 9-13) for;  
analyzing the correlated defect information and position information to  
detect extended objects (Col. 13, lines 60-65, cluster corresponds to extended objects; Col. 15, lines 44-46, i.e., precise location and size of defects corresponds to correlating defect information and position information);  
analyzing the extended objects for repetition across the substrate (Col. 13, lines 60-65, i.e., the **clusters** of defect are highlighted on the wafer map).

As for claims 19-20, respectively, **Dor** further discloses,

- the substrate is **at least one of** a semiconductor substrate, a reticle, and a mask (Col. 15, lines 18-20, wafer corresponds to semiconductor substrate);

- the sensor is an optical sensor (Col. 6, lines 5-15).

However **Dor** does not specifically disclose some limitations of claim 17, but

**Ninomiya** discloses such limitations as follows:

- a stage for providing relative movement between the sensor and the substrate (Fig. 2, stage controller 15); and correlating defect information from the sensor and position information from the stage (Fig. 6, Step 604, i.e., determining unit 101 calculates a correlation between selected defects' position-coordinates 104 and position coordinates 4; Page 6, [077], lines 13-15, i.e., the defects position-coordinates 4 in the coordinate system xy are caused to correspond to stage control information from a stage controller; Page 4, [0058], lines 1-3, i.e., unit 29 calculates the defect's position-coordinates 104 from the electro-beam' position information; Page 4, [0048], lines 14-20; Page 7, [0082], lines 8-13).

Therefore, it would have been obvious to a person of the ordinary skill in the art at the time the invention was made to combine the defect source identifier of **Dor** with the inspecting defect and system of **Ninomiya** because it would provide an improved inspection system that correlates defects' position coordinates between the apparatuses (**Ninomiya**, Abstract).

3. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dor et al. (US 6,701,259)** in view of **Meisburger et al. (US 5,502,306)**.

Regarding claims 3-5, **Ninomiya** discloses the limitations of claim 1 above but fail to disclose the limitations of claims 3-5. However, **Meisburger** discloses the limitations of claims 3-5, respectively, as follows:

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- the substrate is a monolithic semiconducting substrate having integrated circuitry thereon (Col. 9, lines 63-68; Col. 3, lines 7-8; Col. 1, lines 10-12);
- the substrate is a reticle (Col. 1, line 23);
- the substrate is a mask (Fig. 1, element 57).

Therefore, it would have been obvious to a person of the ordinary skill in the art at the time the invention was made to combine the inspecting defect system of **Dor** with the inspection system of **Meisburger** because it would provide an improved and accurate automatic inspection of substrate of various descriptions used in the making of micro-circuits (**Meisburger**, Abstract, lines 12-14; Col. 1, lines 10-12).

4. Claims 7-10, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dor et al. (US 6,701,259)** in view of **Michael et al. (US 6,167,150)**.

Regarding claim 7-10 , 13-16, **Dor** discloses the limitations of claims 1 , 11 above. However, **Dor** fails to disclose the limitations of claims 7-10, 13-16. But **Michael** discloses such limitations as follows:

Regarding claims 7-8 and 13-14,

- specifying a bounding box size (Col. 6, lines 27-33).

As for claims 9 and 15,

- specifying a bounding box orientation (Col. 9, lines 25-33; Fig. 13).

As for claims 10 and 16,

- specifying a bounding box overlap (Figs. 14A-14C, bounding box 1420 is added or overlapped with image 1410).

Therefore, it would have been obvious to a person of the ordinary skill in the art at the time the invention was made to combine the inspection system of **Dor** with the method for detecting extended defects in an object as taught by **Michael** because it would provide an improved defect detection system for automatically detecting extended defects in a surface of an object using magnitude and the orientation of the edges or boundary in the image (**Michael**, Col. 2, lines 38-42).

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Dor et al. (US 6,701,259)** and **Ninomiya (US 2002/0035435 A1)** in view of **Michael et al. (US 6,167,150)**.

Dor and Ninomiya disclose the limitations of claim 17 above but fails to disclose the limitations of claim 18. However, Michael discloses such limitations as follows:  
As for claim 18,

- an input for receiving at least one of a bounding box size, a bounding box orientation, and a bounding box overlap as adjustable parameters for use in detecting and analyzing the extended objects for repetition (Col. 6, lines 27-33; Fig. 8, bounding box 840).

Therefore, it would have been obvious to a person of the ordinary skill in the art at the time the invention was made to combine the inspection system of **Dor and Ninomiya** with the method for detecting extended defects in an object as taught by **Michael** because it would provide an improved defect detection system for automatically detecting extended defects in a surface of an object using magnitude and the orientation of the edges or boundary in the image (**Michael**, Col. 2, lines 38-42).

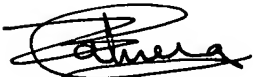
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***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning communication or earlier communication from the examiner should be directed to Zoila Cabrera, whose telephone number is (571) 272-3738. The examiner can normally be reached on M-F from 8:00 a.m. to 5:30 p.m. EST (every other Friday).

If attempts to reach the examiner by phone fail, the examiner's supervisor, Leo Picard, can be reached on (571) 272-3749. Additionally, the fax phones for Art Unit 2125 are (703) 872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist at (703) 305-9600.



Zoila Cabrera  
Patent Examiner  
7/11/05